Please replace paragraph **[0089]** as follows:

[0089] Furthermore, in order for the underfill material 23 to properly permeate to the bonded portion of the bumps 4, the second layer 5 on which the AT-cut quartz crystal resonator 6 is mounted may include two layers, i.e., a first layer 24 and a second layer 25. The opening portion of the first layer 24 is formed to be larger than the opening portion of the second layer 25. By forming the second layer 25 in such a manner, the underfill material 23 properly permeates to the bonded portion of the bumps 4 and a highly reliable bonding structure is obtained.

Please replace paragraph **[0107]** as follows:

[0107] In this embodiment, the vibration direction US2 of the ultrasonic waves for ultrasonic bonding and for forming bumps on the IC chip 2 shown in Fig. 15, and vibration direction US1 of the ultrasonic waves for performing a ultrasonic bonding of the IC chip 2 and the base 1 shown in Fig. 14 are set to be different, preferably, in directions which differ from one another by 90 degrees.

IN THE CLAIMS:

Please replace claims 1-5, 7-17 and 19-30 as follows:

1. (Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit having a plurality of bumps formed thereon; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

the semiconductor integrated circuit being mounted in a center of an opening formed in a center of a base, and the semiconductor integrated circuit being connected to an input/output electrode pattern on the base through the plurality of bumps.

2. (Amended) The piezoelectric device according to claim 1, the plurality of bumps formed on the semiconductor integrated circuit being formed at regular intervals on a center portion of an active element surface of the semiconductor integrated circuit.

3. (Amended) The piezoelectric device according to claim 1, the plurality of bumps formed on the semiconductor integrated circuit being concentrically formed about a center of an active element surface of the semiconductor integrated circuit.

4. (Amended) The piezoelectric device according to claim 1, further comprising a dummy bump formed on an active element surface of the semiconductor integrated circuit.

5. (Amended) The piezoelectric device according to claim 4, the dummy bump formed on the semiconductor integrated circuit being connected to the electrode pattern on the base.

7. (Amended) The piezoelectric device according to claim 1, each of the plurality of bumps formed on the semiconductor integrated circuit being shaped to have two levels, a first level having a diameter 0.8 to 0.9 times and a second level having a diameter 0.4 to 0.45 times a length of a side of an opening in a pad provided on an active element surface of the semiconductor integrated circuit.

8. (Amended) The piezoelectric device according to claim 1, the base comprising a ceramic composite substrate.

9. (Amended) The piezoelectric device according to claim 1, each of the plurality of bumps formed on the semiconductor integrated circuit being an Au bump.

10. (Amended) The piezoelectric device according to claim 1, a protrusion being formed in at least one side wall of the base facing the side of the semiconductor integrated circuit.

11. (Amended) The piezoelectric device according to claim 10, the protrusion being formed in each of side walls of the base facing two sides along the longitudinal direction of the semiconductor integrated circuit.

12. (Amended) The piezoelectric device according to claim 10, the protrusion formed in the side wall of the base having a substantially same height as, or is higher than, the semiconductor integrated circuit.

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13. (Amended) The piezoelectric device according to claim 10, wherein a gap between the protrusion formed in the side wall of the base and the semiconductor integrated circuit being set to a range between 0.05 and 0.15 mm.

SUB C2

14. (Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

a plurality of bumps being formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit being mounted in an opening formed in a center of a base, and the semiconductor integrated circuit being connected to an input/output electrode pattern of the base through the plurality of bumps.

15. (Amended) The piezoelectric device according to claim 14, the plurality of bumps formed on the semiconductor integrated circuit being formed at regular intervals at a center portion of the active element surface of the semiconductor integrated circuit.

16. (Amended) The piezoelectric device according to claim 14, further comprising a dummy bump formed on the active element surface of the semiconductor integrated circuit.

17. (Amended) The piezoelectric device according to claim 16, the dummy bump formed on the semiconductor integrated circuit being connected to the electrode pattern on the base.

19. (Amended) The piezoelectric device according to claim 14, each of the plurality of bumps formed on the semiconductor integrated circuit being shaped to have two levels, a first level having a diameter 0.8 to 0.9 times and a second level having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

20. (Amended) The piezoelectric device according to claim 14, the base comprising a ceramic composite substrate.

21. (Amended) The piezoelectric device according to claim 14, the plurality of bumps formed on the semiconductor integrated circuit being Au bumps.

22. (Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

a plurality of bumps being formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit being mounted in a center of an opening formed in a center of a base, and the semiconductor integrated circuit being connected to an input/output electrode pattern through the plurality of bumps by ultrasonic bonding.

23. (Amended) The piezoelectric device according to claim 22, a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit being

perpendicular to two opposing sides of the active element surface of the semiconductor integrated circuit at which the plurality of bumps are formed.

24. (Amended) The piezoelectric device according to claim 22, a printing direction of the electrode pattern on the base being the same as a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit.

25. (Amended) The piezoelectric device according to claim 22, each of the plurality of bumps formed on the semiconductor integrated circuit being shaped to have two levels, a first level having a diameter 0.8 to 0.9 times and a second level having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

26. (Amended) The piezoelectric device according to claim 25, each of the plurality of bumps formed on the semiconductor integrated circuit being shaped to have two levels, a first level being 80 to 90 μm in diameter and 30 to 35 μm in height, and a second level being 40 to 45 μm in diameter and 30 to 35 μm in height.

27. (Amended) The piezoelectric device according to claim 22, the base comprising a ceramic composite substrate.

28. (Amended) The piezoelectric device according to claim 22, the plurality of bumps formed on the semiconductor integrated circuit being Au bumps.

29. (Amended) The piezoelectric device according to claim 22, a longitudinal direction of the electrode pattern on the base being the same as a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit.

30. (Amended) The piezoelectric device according to claim 22,

a vibration direction of ultrasonic waves for ultrasonic bonding and for forming bumps on the semiconductor integrated circuit being different from a vibration

REMARKS

Claims 1-32 are pending. By this Amendment, the specification and claims 1-5, 7-17 and 19-30 are amended for further clarity. No new matter is added.

The attached Appendix includes marked-up copies of each rewritten paragraph (37 C.F.R. 1.121(b)(iii)) and claim (37 C.F.R. 1.121(c)(ii)).

In view of the foregoing amendments and remarks, Applicant submits that this application is in condition for initial examination. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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JAO:EDM/zmc

Attachments:
Substitute Abstract
Appendix

Date: April 06, 2001

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DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461